MA780 MULTIPORT MEMORY

digital

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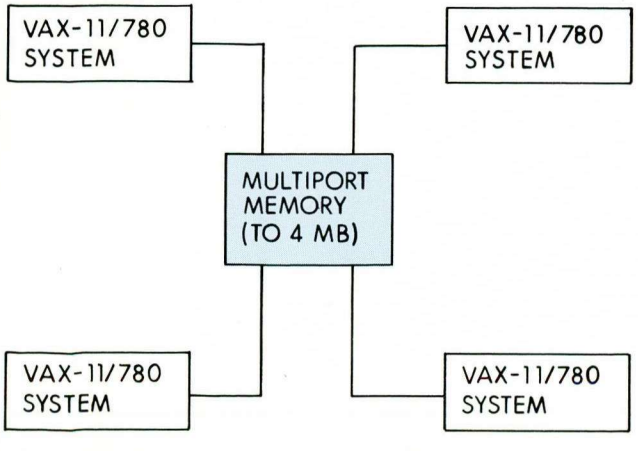
The MA780 multiport memory enables up to four VAX-11/780 processors to share a bank of from 256 kilobytes to 2 megabytes of memory. This capacity allows VAX-11/780 users to develop multicomputer configurations for very high throughput or enhanced-availability applications.



FEATURES

Capacity and Expandability

- Expandable in 256-kilobyte increments to 2 megabytes per shared memory bank
- Two MA780s (up to 4M bytes) supported per processor
- Up to four VAX-11/780 processors can share each MA780
- Expands VAX-11/780 address space up to a system total of 12M bytes of physical memory
- Can be field installed on existing VAX-11/780 systems

Throughput

- Full random access read/writes from all ports
- Unique port servicing algorithm minimizes port wait time
- 11M bytes per second maximum total throughput on transfers to memory
- 700-nanosecond memory cycle time for 64 transfers
- Data/command input and output buffer for each port

Data Integrity

- Memory error correcting code (ECC) corrects all single-bit errors and detects all double-bit errors on reads/writes
- Interlock capability prevents a shared memory location from being read by one processor while being updated by another
- Invalidation logic enables caching of shared memory data
- Parity for error-checking on all internal MA780 buses

Failsoft Capability and Maintainability

- Generates interrupts to notify ports of power failures and error conditions as soon as detected. Interrupts aid in rapid diagnosis and repair and can be used in the development of failsoft software
- Each port can be separately switched off line, and the associated CPU can be powered down or repaired with the balance of the system on-line
- Extensive diagnostics allow rapid testing of the system from a single port

Application Flexibility

- One port can pass an interrupt directly to any other port, providing rapid interprocessor communication
- Each port can specify its own starting address as needed by its application software

DESCRIPTION

The MA780 multiport memory is a bank of MOS semiconductor memory with Error Correcting Code (ECC) that can be shared by up to four VAX-11/780 systems. Each system can randomly access all of the shared memory in exactly the same way it accesses its local memory.

Each MA780 can be expanded from a minimum of 256K bytes to a maximum of 2M bytes. This storage is in addition to each system's local memory, which can be as large as 8M bytes. Since there can be up to two MA780s connected to a CPU, a VAX-11/780 system can now directly address up to 12M bytes of physical memory.

Extensions to VAX/VMS make access to the shared memory transparent to the programmer. An application built around multiple cooperating processes can be reconfigured to run on a multi-CPU system with no program modification. Processes can be moved from one CPU to another with transparency to the programs involved.

The MA780 can be thought of as a very fast communication device between VAX-11/780 systems. Specifically, VAX/VMS provides support for interprocessor communications through the sharing of data regions, VMS mailboxes, and common event flags. VAX/VMS also allows code to be shared among CPUs.

The sharing of data regions has been achieved through extensions to the "global sections" capability of VMS. Global sections provide named, protected areas of memory that can be shared selectively among user programs. The extension of this facility to shared memory is totally upward compatible with the use of global sections in local memory.

An additional extension to VMS, logical name translation, has been made for global section, mailbox and common event flag names. It allows the restructuring of applications to execute with no program modification in multicomputer environments.

The mailbox is the fundamental message-oriented interprocess communication mechanism in VMS. It is a record-oriented "virtual" device with dynamic buffering that provides excellent performance for multicomputer systems. Since there is very little overhead and an error-free data transfer path, messages are transmitted at memory speeds. The maximum storage space for messages in each mailbox is 64K bytes. Messages can be of any length up to 64K bytes. As with shared data areas and common event flags, extensions to the mailbox facility allow the placement of mailboxes in shared memory.

Common event flags provide a simple, fast mechanism for one process to synchronize itself with other processes. A process can set, clear, test and wait for an event flag or a combination of event flags.

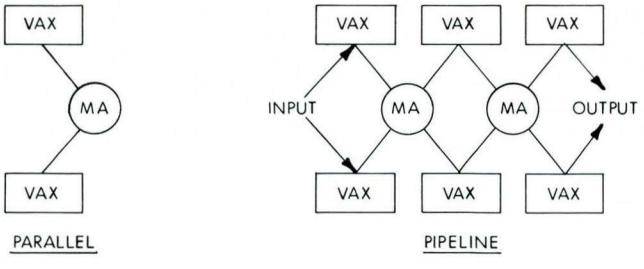
Shared memory global sections can also contain sharable code. Images that have been developed to run in local memory can be easily redirected to shared memory, simply by making the appropriate logical name assignments before installing them on-line. The shared memory not required for interprocessor communication can be used to off-load some of the shared code from local memory.

In multicomputer systems, MA780 memory does not contain any of the VMS system code. Each system must have local memory to run its own copy of VMS. Thus each system remains independent even though it is connected to the multiport memory.

Applications

The ability to share data and code between processors reduces overall memory requirements. It can also enhance a system's performance and uptime in ways that are vital to many applications. Such applications usually require very fast inter-processor communication plus as much isolation between systems as possible. This isolation is necessary so that a failure in any one of the systems will have little or no effect on the total configuration. The MA780 provides many features for the implementation of high-availability systems, such as separate on-line, power-down of a port and its associated CPU. Also, the inherent error detection and parity-checking features of the VAX-11/780, VAX/VMS and the MA780 provide the high level of data integrity which is necessary in these systems.

The MA780 can be used to configure multiple computer systems for very high throughput. Depending on the application, the CPUs can be arranged in either a parallel or pipeline manner, as shown below:



In parallel systems, two or more appropriately programmed CPUs can divide a task. This allows the CPUs to effectively pool their power to finish the job extremely quickly. Pipeline systems can increase throughput by allowing instantaneous data exchange between CPUs that are handling sequential parts of an application.

Performance and Operation

The MA780 can provide total throughput at up to 11M bytes per second. This performance is possible because each port has a buffer for commands and data. The MA780 controller services ports on a demand basis, so no time is wasted in polling inactive ports. A servicing algorithm guarantees that no port waits more than 3 memory cycles to gain access to the shared memory.

The MA780 has been designed to virtually eliminate stale data in the CPU caches. After a write to a shared memory location, the MA780 sends an invalidate signal to all CPUs. This signal transmits an address to the CPUs. Each CPU's cache then checks to see if it contains that address. If so, it marks the contents as invalid. On subsequent reads by the CPU, this invalidation forces the CPU to seek the new information from shared memory. The VAX-11/780 cache therefore retains its transparency to software.

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For multicomputer systems where there is considerable traffic on a system's SBI, a selective cache invalidation option, the MA780-D, is available. It is called an "invalidation map" and is useful primarily in systems with three or four CPUs. It causes the MA780 to send invalidate signals only to those CPUs that have accessed a given location in shared memory. Its operation is quite straightforward: the MA780-D has one entry for each 64-bit quadword in shared memory. This entry contains four bits, one for each CPU. Whenever a CPU reads a 64-bit quadword from shared memory, the MA780 controller sets the bit in the correct invalidation map entry. The next time a CPU writes into that 64-bit quadword, the MA780 controller notifies only those CPUs whose bits have been set in the invalidation map. Once that is done, all the bits are cleared except that of the CPU performing the write operation. In this way, the overall traffic on all SBIs and cache activity is kept to a minimum while data integrity is still maintained.

TECHNICAL SPECIFICATIONS

MECHANICAL

Dimensions
60″ H X 26″ W X 30″ D
152.4 cm H X 66 cm W X 67.2 cm D

Weight
500 lbs. (227 kg)

Packaging

A single-width H9602 cabinet holds one or two MA780s. Each MA780 includes multiport memory controller, 256K bytes of MOS memory, two port interfaces, and power supply. A fully expanded MA780 holds 2M bytes of memory. One cabinet can thus hold 4M bytes of multiport memory.

ELECTRICAL

Input Power
60 Hz, 115 Vac, 30 amps
50 Hz, 230 Vac, 15 amps

Hardware Prerequisite
VAX-11/780 system with mounting space in either the basic CPU cabinet or in the VAX-11/780 CPU expander cabinet for the port interfaces.

ENVIRONMENTAL

Temperature
Operation: 60–90°F (15–32°C)
Storage: 40–112°F (5–45°C)

Relative Humidity
Operative: 20–80%

Storage: 5–48%

OPERATIONAL

Memory Type
16K bit MOS with Error Correcting Code (ECC)

Memory Capacity
256K bytes included
256K bytes increments (standard VAX-11/780 memory)
Up to 2M bytes per MA780

Basic Word Size of Memory Array
64 bits (8 bytes) plus 8 bits ECC

Memory Cycle Time per 64 bits
700 nanoseconds

Battery Backup (optional)
10 minutes for 2M bytes (H7112-A/B)

Number of ports
2 to 4
Can be upgraded on site

Port Arbitration
Demand basis with servicing algorithm guarantees that a port waits no longer than 3 memory cycles to gain access to the shared memory.

PERFORMANCE

Maximum Throughput
(Reads/Writes with all ports active) 11M bytes/second*

* Rate applies to 64-bit data transfers; smaller-size transfers will result in lower throughput.

Also note that throughput to shared memory as seen by a CPU is very much a function of other factors within that processor (i.e., CACHE hits, I/O traffic, SBI traffic, etc.).

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